REMARKS

Applicants have carefully reviewed and considered the Office Action mailed on September 19, 2007. Reconsideration is respectfully requested in view of the foregoing amendments and the comments set forth below.

By this Amendment, claims 1, 10, 21 and 24 are amended. Accordingly, claims 1-7, 9-14, and 16-26 are pending in the present application.

Claims 10 and 21 were objected to because of the informalities indicated in the middle of page 2 of the Action. The foregoing amendments to claims 10 and 21 address the informalities noted by the Examiner. Accordingly, it is believed that the informalities have been resolved. Withdrawal of the claim objections is respectfully requested.

Claims 1-6, 9-13, 16-17, 21 and 23-26 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Application Publication No. 2006/0206738 to Jeddeloh et al. (hereinafter referred to as "Jeddeloh") in view of U.S. Patent No. 5,995,434 to Ryu. This rejection is respectfully traversed.

Jeddeloh is directed to a system and method for selective memory module power management. According to the Examiner, the recited "chip" of the claimed invention is a memory module 504. While a memory module may be a chip in the broad sense, their operation is different from logic devices or electrical components which the claimed invention targets. In particular, Jeddeloh discloses reduced power, but does not mention the word "speed", let alone an idle state when the power is turned on (that is, active so that the operating performance of the chip is maintained) based on component speed characteristics as claimed in the present application. While the secondary reference to Ryu uses the word "speed", there is a different meaning of the term "speed" than the meaning of "component

speed" as defined in paragraph [00014] of the originally filed specification of the present application.

The Examiner in the Action appears to equate inactivity of a chip with determining the threshold temperature based on speed characteristics of the chip as paragraph [0029] of Jeddeloh teaches:

> Once the temperature sensor 370 detects that the threshold or thresholds have been reached, the temperature sensor 370 might signal the power management controller 360 that the temperature level indicates the memory module 300 has not been actively used, and could assume a reduced power state.

According to the Examiner, the "threshold temperature is based on 'speed characteristics' of the chip at the threshold temperature" because "the memory module has not been actively used for a long time". That is, there is no speed if the memory module has not been used. But, it is respectfully submitted that Jeddeloh bases its threshold activity on inactivity and not the recited speed characteristics of the chip as defined in paragraph [00014] of the originally filed specification of the present application and set forth in the claimed invention.

For example, in memory devices like the applied references, one of ordinary skill in the art would understand that the recitation of "speed" refers to how many bits of information can be read/written at the unit of time, (e.g, second). On the other hand, in logic devices and the claimed invention the term "speed" is defined as the propagation delay of electrical signals within an electrical component. The propagation delay may be referred to as transistor speed or switching speed.

If a memory module is made of several memory chips (as in Jeddeloh), the larger the number of memory chips connected to the memory module, the more information

could be stored and read/written. In other words, with more memory chips attached to the module, the higher the speed (how many bits of information can be read/written at a unit of time) of the memory module. If there is no need for large amounts of information, then the "memory speed" can be reduced. The reduction of the memory speed is achieved by reducing the number of memory chips attached to the memory module or turning OFF the power of the memory chips as taught by Jeddeloh. That is, Jeddeloh discloses a device component performance is not maintained as required by the claimed invention because the device is turned OFF.

In fact, paragraphs [0023]-[0029] of Jeddeloh teach turning off the power from some of the memory chips, if only a part of the memory module is needed. The Examiner appears to be referring to the turning OFF of some of the memory chips as "reduced speed". It is respectfully submitted that Jeddeloh only teaches if the temperature of the memory chip goes down below a predetermined value (representing inactivity), the memory module can operate at "reduced speed" by turning of some of the memory chips. This is not the claimed invention. No where does Jeddeloh disclose determining the threshold temperature based on "component speed" characteristics of the chip where the minimum allowed voltage and the threshold temperature maintain the speed characteristics of the chip, while providing significant reduction in power consumption of the chip as recited in independent claims 1, 10, 21 and 24.

To the contrary, Jeddeloh does not disclose a memory chip where the minimum allowed voltage (power turned OFF) and the threshold temperature **maintain** the speed characteristics of the chip. As explained above, the memory speed of the chip is reduced as the number of memory chips attached to the module is turned off or lessened. That is,

Jeddeloh teaches against maintaining the speed characteristics of the chip (in the memory sense) and does not address the component speed characteristics set forth in the independent claims.

As defined in paragraph [00014] of the originally filed specification of the present application, claimed term "component speed" means inherent transistor speed, also called switching speed of the chip. It is a fundamental characteristic of a transistor demonstrating how fast it can charge or discharge a capacitor (or output logic gate). In other words, how large could the electrical current be that a transistor (or component) supplies.

Physically the component speed depends on many parameters, however, in claimed invention we concentrate on two parameters: temperature and voltage. At modern VLSI technologies, the lower the temperature, the higher is the electron mobility and the faster is the transistor speed. Note that in that physical phenomenon transistor speed is increasing with temperature decrease. This is exactly opposite to what is mentioned by Jeddeloh and by Examiner in his Action: the memory speed is decreasing when temperature decreases. Why? Because in Jeddeloh the speed pertains to the number of bits that are read/written by the memory. The smaller number of read/write operations, the less active is the memory and, as a result, the memory temperature is lower.

As argued above (and as described in the Description of the Invention), the claimed invention employs the physical phenomenon of change of transistor or component speed as a function of temperature in order to reduce overall logic chip power consumption. This physical phenomenon is not mentioned neither in either Jeddeloh nor

Ryu. In other words, the applied memory devices are not utilizing this phenomenon at all and therefore are not relevant to the claimed invention.

The secondary reference to Ryu was applied for its teaching of a system where the operating voltage of a self-refresh is lower than that of the normal mode. The "component speed" defined in paragraph [00014] and recited in the claims is not addressed in Jeddeloh, and while the word "speed" is used in the background of Ryu, Ryu fails to disclose a threshold based on the propagation delay of electrical signals within an electrical component. Instead, Ryu proposes to reduce voltage during a memory re-fresh cycle, which is not relevant to the claimed invention. Considering the memory operation in more detail: memory operation includes reading, writing and storing the data. During storing, the data must be re-freshed in order to avoid its disappearance. Ryu proposes to use a smaller voltage level for re-freshing operation. It is specific to memory module only and not directed to the elements missing from Jeddeloh as argued above.

As described in the specification of the present application, performance control of electrical devices is achieved in order to significantly reduce power lost due to leakage current when the voltage of the electrical component is reduced as low s it cam be without compromising on performance. See paragraph [0016] of the present application. Thus, the claimed invention is in an active state (power is ON) when the device is performing one or more of its specified functions/features. For example, when a device is performing all its functions/features at the highest rate, it generally will consume its highest power and have its highest temperature. If the device performs only certain functions (i.e., not all of them), its power consumption and temperature will be lower. If

not all the functions/features are being used (due to customer application/condition), the device will have a lower power and a lower temperature. This is where the claimed invention can be beneficially applied.

The recited idle/low power state of the claimed invention is an active state (chip is powered ON) where the device is performing a minimum of its specified functions, or waiting. For example, types of device may be a communications device waiting for the next communication session/communication package, a computer placed in the stand-by mode, a device after a math computation has been completed where the device is waiting for the next input. These are examples of devices where possible the lowest power consumption and the lowest device temperature. In all of the above examples, the communications device, the computer and the math computation device are all powered ON in the active state, although in a low power state.

Alternatively, the device temperature could be lower than planned because of a better cooling condition (e.g., higher fan speed than planned by the designer) at the customer platform, a lower ambient temperature at the customer (operated in a colder room than planned by the designer), or the device is closer to the fan at the customer board/card (than planned by the designer). Consequently, the device is provided with better cooling. This is another area where the claimed invention could be beneficially applied.

It is unclear how one of ordinary skill in the art employing common sense would consider modifying Jeddeloh, which proposes switching off the voltage of part of the memory chips in the memory module, to determine a threshold temperature based on component speed characteristics of the chip as defined in paragraph [00014] of the

present application. Contrary to using speed characteristics to determine the threshold temperature, Jeddeloh uses temperature as an indicator that the memory module can turn OFF some of the attached memory chips. That is, if the temperature is lower than the predetermined value, then memory module is not fully active and part of it could be switched off. Jeddeloh's disclosure is not concerned with determining the threshold temperature based on the propagation delay of the electrical signals within an electrical component as defined and claimed by Applicant.

The claimed invention is absolutely different from the applied teachings of Jeddeloh and Ryu. Contrary to the Examiner's understanding of the recited term "speed" in the claimed invention, the threshold temperature is used as an indicator of transistor or component speed (not memory speed). If the chip temperature goes down, the chip voltage could be reduced, but the electrical signals within the chip will come on time and chip will be fully functional ("the minimum allowed voltage and the threshold temperature maintain the component speed characteristics of the chip", as set forth in the independent claims of the present application. Voltage is another modulator of transistor or component speed, the lower the voltage, the slower is the transistor speed and the slower are signals propagating within the chip. Therefore, when temperature goes down, the transistor voltage can be reduced (but according to the claimed invention, the voltage is not switched off - if it is switched off transistor will not operate at all), while transistor or component speed remains the same. Therefore, there is no impact on functionality. The device is still fully functional while its voltage is reduced. This phenomenon is relevant to active states as well as idle states or low power states, when it can provide significant benefits as described in the invention.

It is respectfully submitted that one of ordinary skill in the art would not reasonably combine Jeddeloh and Ryu to achieve the claimed invention in that neither Jeddeloh nor Ryu disclose teach or suggest 1) determining the threshold temperature based on "component speed" characteristics of the chip 2) where the minimum allowed voltage and the threshold temperature maintain the speed characteristics of the chip, while providing significant reduction in power consumption of the chip as recited in independent claims 1, 10, 21 and 24. Further, both Jeddeloh and Ryu disclose turning off memory modules to reduce power. Accordingly, even if combined, the claimed invention would not result. Withdrawal of the rejection of claims 1-6, 9-13, 16-17, 21 and 23-26 under 35 U.S.C. §103(a) is respectfully requested.

Claims 7 and 14 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Application Publication Jeddeloh in view of Ryu and further in view of U.S. Patent No. 6,047,248 to Georgiou et al. (hereinafter referred to as "Georgiou"). Claims 18-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh in view of Ryu and further in view of U.S. Patent No. 5,502,838 to Kikinis and further in view of U.S. Patent No. 6,047,248. These rejections are respectfully traversed.

Georgiou is directed to a performance-temperature optimization by cooperatively varying the voltage and frequency of a circuit. There is no discussion of an idle state or a power down condition. Thus, Georgiou fails to provide the elements missing from Jeddeloh combined with Ryu, as argued above. Accordingly, Georgiou, even if combined with Jeddeloh and Ryu cannot render the claimed invention obvious. Likewise, Kikinis does not disclose the elements missing from the combination of Jeddeloh and Ryu. Withdrawal of these rejections are requested.

In view of the foregoing amendments and remarks, it is respectfully requested that the rejections of record be withdrawn and that a Notice of Allowance be issued indicating that claims 1-7, 9-14, 16-21 and 23-26 are allowed over the prior art of record.

Should the Examiner believe that a conference would advance the prosecution of this application, the Examiner is encouraged to telephone the undersigned counsel to arrange such a conference.

Respectfully submitted,

Date: January 18, 2008

Catherine M. Voorhees
Registration No. 33,074
VENABLE LLP
P.O. Box 34385
Washington, D.C. 20043-9998
Telephone: (202) 344-4000
Telefax: (202) 344-8300

CMV/elw
::ODMA\PCDOCS\DC2DOCS1\913353\1